US007969392B2

(12) **United States Patent**
Yamashita et al.

(10) **Patent No.: US 7,969,392 B2**
(45) **Date of Patent: Jun. 28, 2011**

(54) **CURRENT PROGRAMMING APPARATUS AND MATRIX TYPE DISPLAY APPARATUS**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 1499 days.

(21) Appl. No.: **11/283,862**

(22) Filed: **Nov. 22, 2005**

(65) **Prior Publication Data**

US 2006/0114195 A1 Jun. 1, 2006

(30) **Foreign Application Priority Data**

Nov. 26, 2004 (JP) 2004-342129

(51) **Int. Cl.**
G09G 3/30 (2006.01)
G09G 3/10 (2006.01)

(52) **U.S. Cl.** **345/77**; 315/169.3

(58) **Field of Classification Search** 345/76–83; 313/463; 315/169.3

See application file for complete search history.

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(57) **ABSTRACT**

A matrix type display apparatus includes a pixel circuit unit including electroluminescent elements and pixel circuits driving the electroluminescent elements arranged in a matrix, a plurality of data lines, each corresponding to a column of the pixel circuits for supplying a data current to the pixel circuits, and predetermined current setting circuits for supplying to the data lines a predetermined current for reducing a current to be supplied to the data lines, according to a setting by a reference current unrelated to a displaying, at a time of black displaying of the electroluminescent elements. In addition, switches are arranged corresponding to each of the data lines between the pixel circuits and the predetermined current setting circuits, and a row scanning circuit controls on and off of the switches. The row scanning circuit turns off the switches to disconnect the pixel circuit unit and the predetermined current setting circuits, and sets the predetermined current in the predetermined current setting circuits, and thereafter, the row scanning circuit turns on the switches to connect the pixel circuit unit and the predetermined current setting circuits, and to supply the data lines with the data current and the predetermined current.

3 Claims, 5 Drawing Sheets

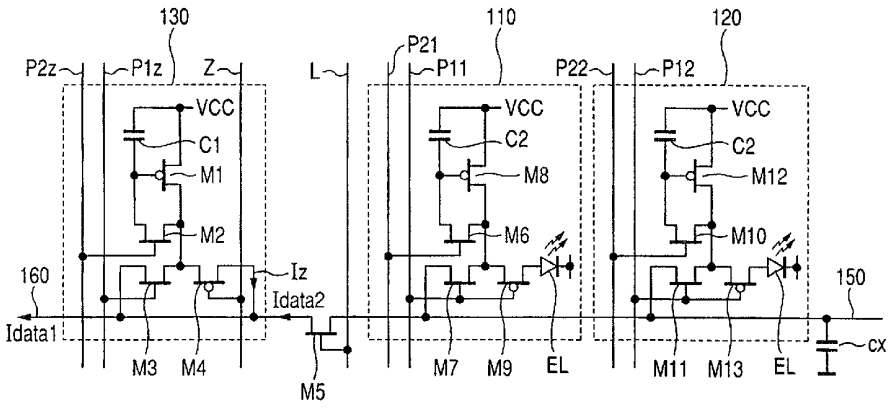

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FIG. 1

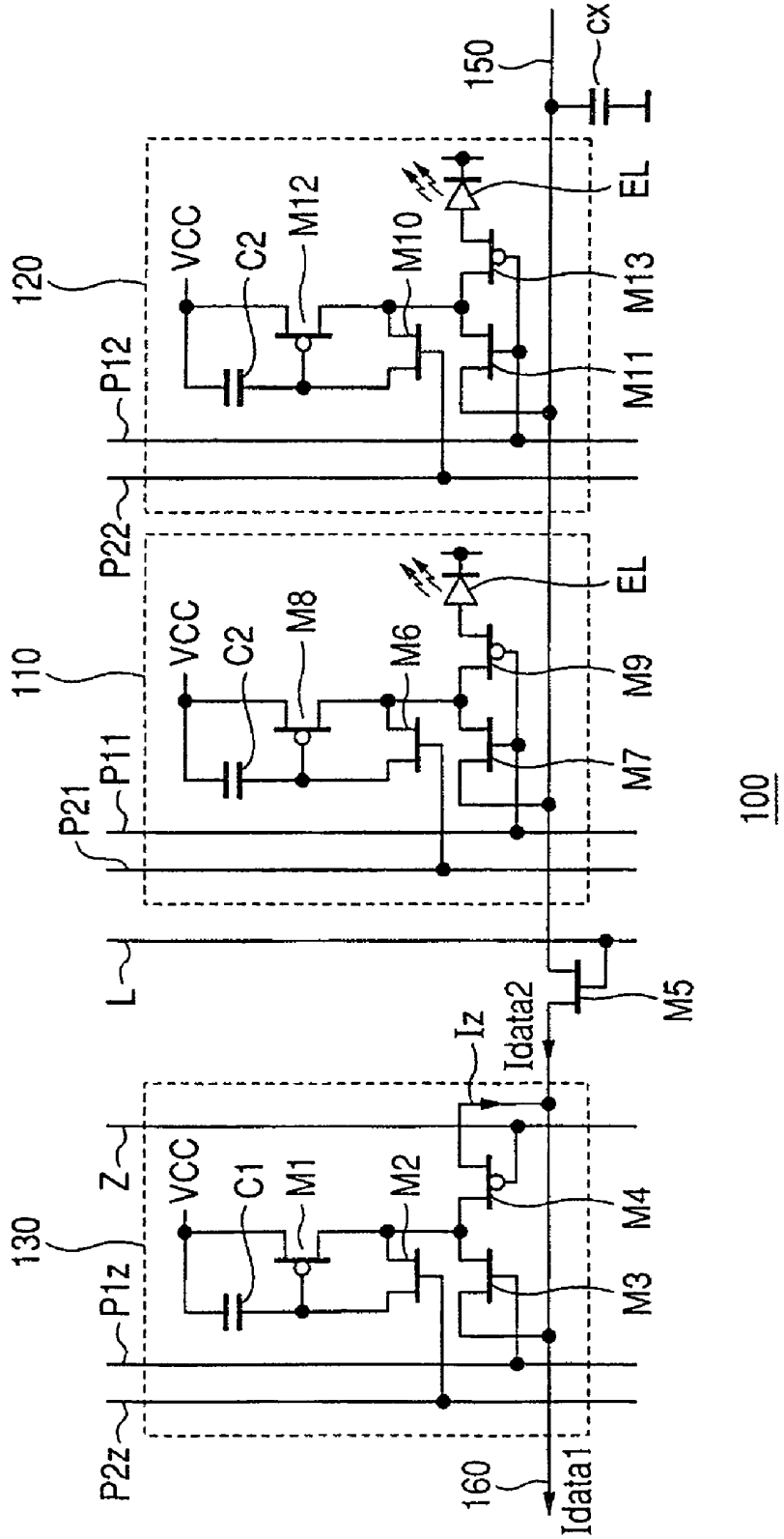

100
110
120
130
150
160
L
Z
P11
P12
P21
P22
P1z
P2z
VCC
C1
C2
M1
M2
M3
M4
M5
M6
M7
M8
M9
M10
M11
M12
M13
EL
CX
Iz
Idata1
Idata2

FIG. 2

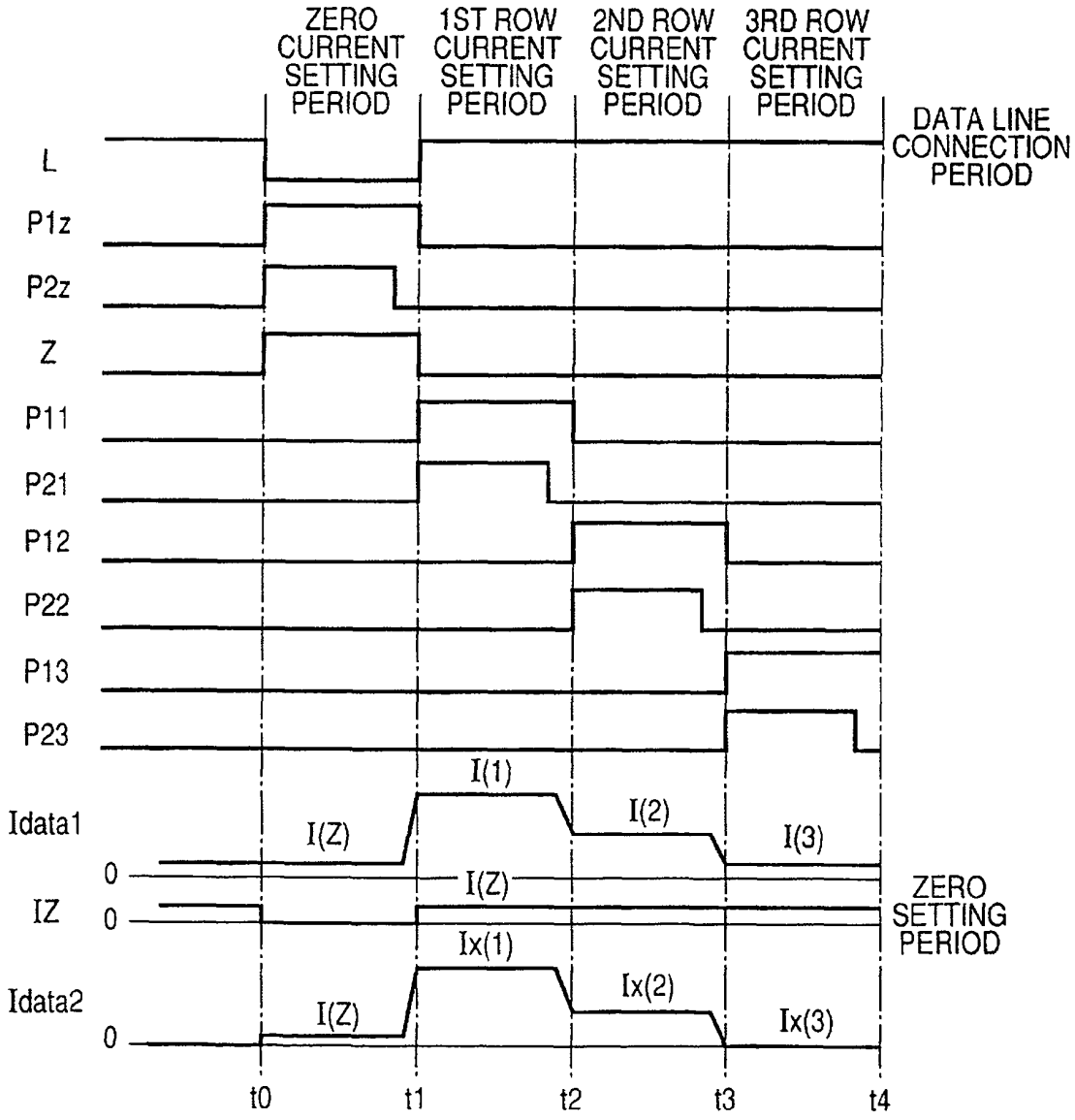

ZERO CURRENT SETTING PERIOD
1ST ROW CURRENT SETTING PERIOD
2ND ROW CURRENT SETTING PERIOD
3RD ROW CURRENT SETTING PERIOD
DATA LINE CONNECTION PERIOD
L
P1z
P2z
Z
P11
P21
P12
P22
P13
P23
Idata1
I(1)
I(Z)
I(2)
I(3)
0
I(Z)
IZ
0
ZERO SETTING PERIOD
Ix(1)
Idata2
Ix(2)
I(Z)
Ix(3)
0
t0
t1
t2
t3
t4

FIG. 3

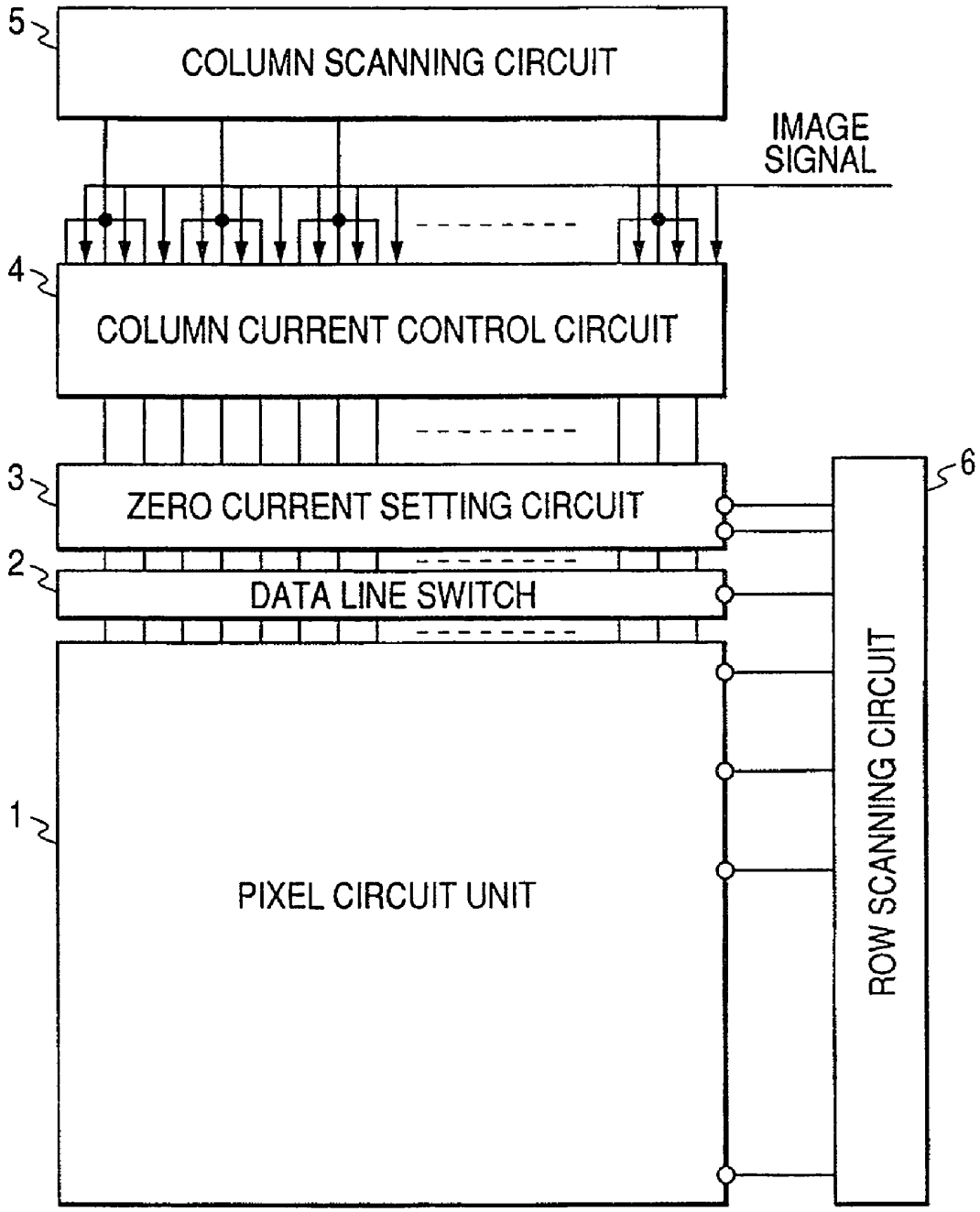

5
COLUMN SCANNING CIRCUIT
IMAGE SIGNAL
4
COLUMN CURRENT CONTROL CIRCUIT
3
ZERO CURRENT SETTING CIRCUIT
6
2
DATA LINE SWITCH
1
PIXEL CIRCUIT UNIT
ROW SCANNING CIRCUIT

FIG. 4

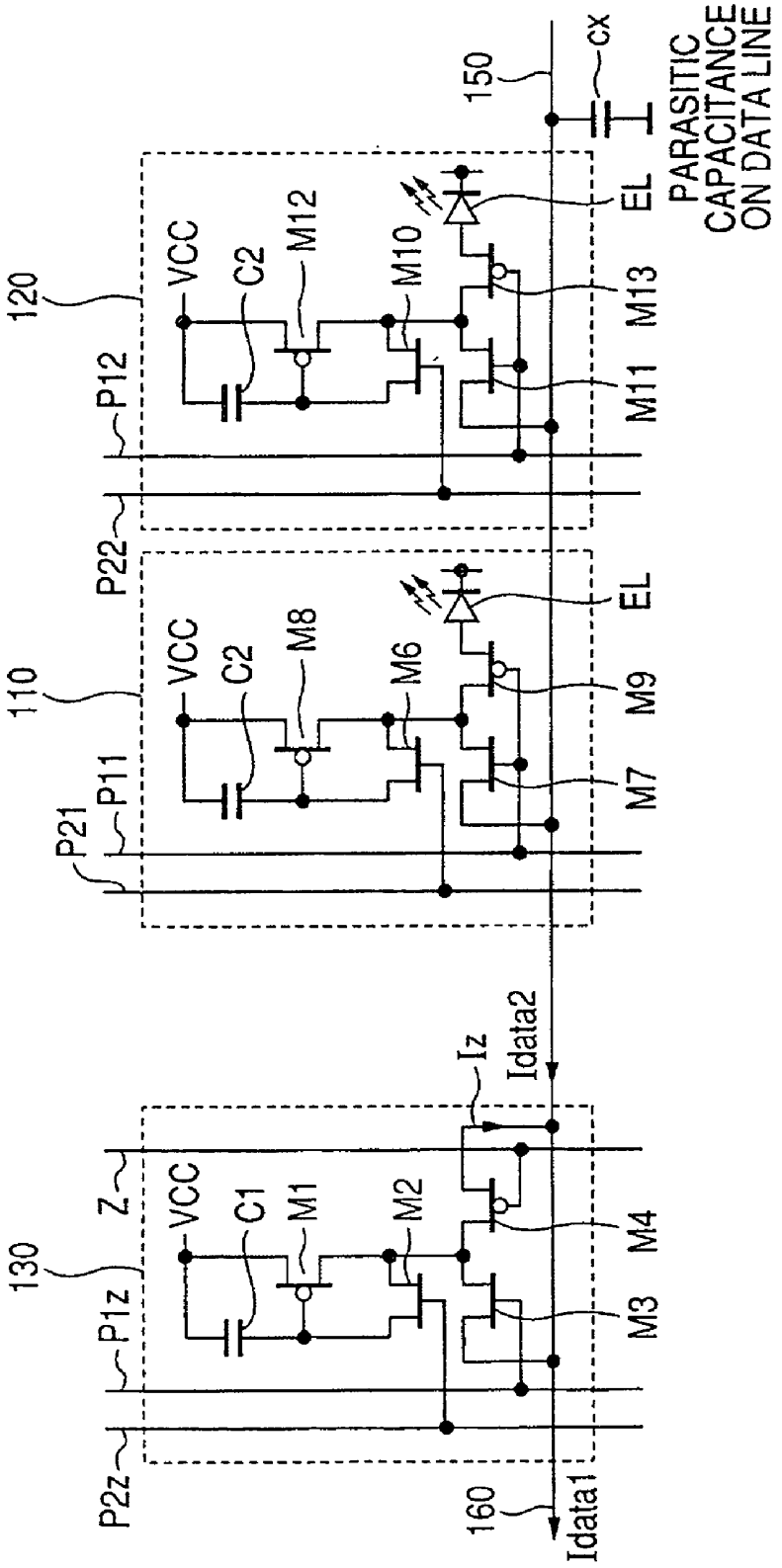
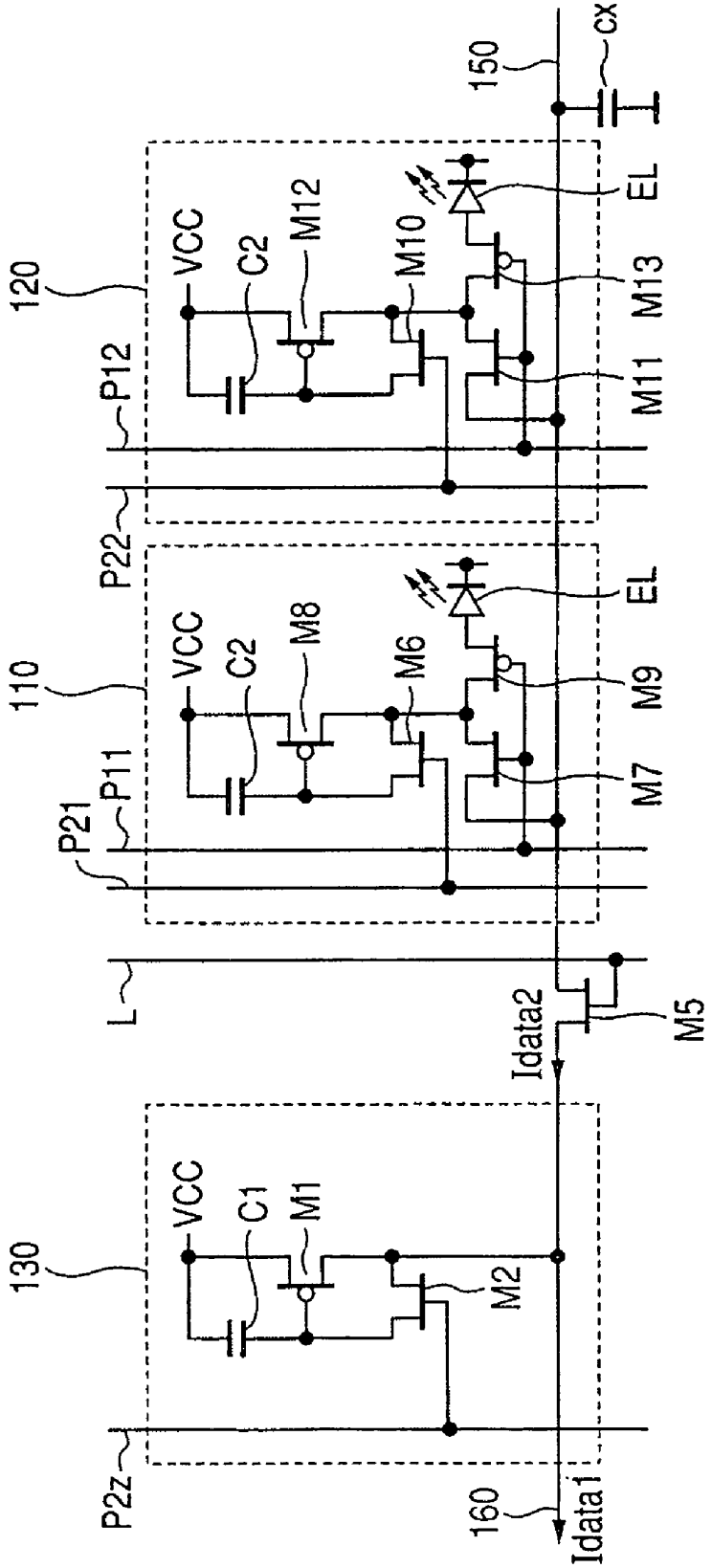

120
P12
VCC
C2
M12
M10
EL
M13
M11
150
CX
PARASITIC CAPACITANCE ON DATA LINE
P22
110
P11
P21
VCC
C2
M8
M6
EL
M9
M7
Iz
Idata2
130
P1z
Z
VCC
C1
M1
M2
M4
M3
P2z
160
Idata1

FIG. 5


150
CX
120
VCC
C2
M12
M10
EL
M13
M11
P12
P22
110
VCC
C2
M8
M6
EL
M9
M7
P11
P21
L
Idata2
M5
130
VCC
C1
M1
M2
P2z
160
Idata1

CURRENT PROGRAMMING APPARATUS AND MATRIX TYPE DISPLAY APPARATUS

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention generally relates to a current programming apparatus, a matrix type display apparatus, a current programming method, and a drive method of a matrix type display apparatus, and more particularly to ones suitably used for an active matrix type display apparatus using current based driven display elements.

2. Description of Related Art

In an active matrix type display apparatus using electroluminescent elements, a current writing type circuit writing a drive current of a light emitting device into the drive circuit of each pixel to make the drive circuit store the drive current has been used. In the present specification, such an operation of writing a drive current into each pixel of a matrix type display apparatus to make the drive circuit store the drive current is called as current programming, and the circuit for the current programming is called a current programming circuit.

In FIG. 18 of United States Patent Published Application No. 2002/0195964, a current programming circuit holding a current flowing in a data line as a gate-source voltage of a transistor is disclosed. Moreover, in the document, it is mentioned that gradation displays of black and low luminance levels can be improved by flowing the current into the direction of cancelling a writing current at the time of writing data into the current programming circuit.

When a conventional current writing type pixel circuit is used, there is a case where an operation of writing an image data current cannot be stably performed in each pixel circuit. The details of the case are described in the following, but the cause of the case is the dispersion of the threshold value of the drive transistor of each pixel.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a current programming apparatus, an active matrix type display apparatus, and a current programming method of these apparatus, all making it possible to perform the writing operation of the image data current mentioned above stably.

A current programming apparatus of the present invention is a current programming apparatus including:

a current source;

a plurality of first circuits commonly connected with a data line, each receiving supply of a data current through the data line;

a second circuit having a terminal connected to the current source; and

a switch electrically connecting or breaking the terminal of the second circuit with or from the data line, wherein

the current source generates a predetermined current and supplies the generated current to the second circuit through the terminal while the switch is off, whereby a value of the predetermined current is written in the second circuit; and

the current source generates a current based on data, and the second circuit generates a current based on the written value of the predetermined current, and a difference current between the current generated by the current source and the current generated by the second circuit is supplied to one of the first circuits through the data line while the switch is on, whereby a value of the difference current is written in the first circuit as a value of the data currents.

A matrix type display apparatus of the present invention is a matrix type display apparatus including:

a current source;

a plurality of display elements arranged in a matrix to be current based driven;

a plurality of pixel circuits each provided to each of the display elements, the pixel circuits commonly connected in column directions with data lines to receive supply of data currents through the data lines;

predetermined current setting circuits having a terminal connected to the current source; and

switches each electrically connecting or breaking the terminal with or from each of the data lines, wherein

the current source generates predetermined currents to supply the generated currents to the predetermined current setting circuits through the terminal while the switches are off, whereby a value of the predetermined currents are written in the predetermined current setting circuits; and

the current source generates a current based on data, and one of the predetermined current setting circuits generates a current based on the written values of the written predetermined currents, and difference currents of the currents generated by the current source and the currents generated by the predetermined current setting circuits are provided to the pixel circuits, whereby values of the difference currents are written into the pixel circuits as values of the currents based on the data.

A current programming method of the present invention is a current programming method including:

a first step of supplying a data current to each of a plurality of first circuits connected to a data line commonly through the data line to write a value of the data current into the first circuits; and

a second step of supplying a predetermined current to a second circuit to write a value of the predetermined current into the second circuit, wherein

the second step includes a step of breaking the second circuit from the data line electrically and a step of making a current source generate a predetermined current to supply the generated current to the second circuit, and

the first step includes a step of connecting the second circuit with the data line electrically, a step of making the current source generate a current based on data, a step of making the second circuit generate a current based on the value of the predetermined current written at the second step, and a step of supplying a difference current of the current generated by the current source and the current generated by the second circuit to one of the first circuits through the data line.

A drive apparatus for driving electro-optic elements of the present invention includes:

a matrix circuit unit (**1**) in which circuits (**110**, **120**) for generating drive currents to be supplied to the electro-optic elements (EL) are arranged in a matrix;

a current source (**4**) for supplying a writing current (Idata**1**) to each of the circuits through one of a plurality of data lines;

a current setting circuit (**130**) for flowing a compensation current (Iz) in a direction of cancelling the writing current in each of the data lines, the current setting circuit provided to each of the data lines; and

switches connecting or breaking the current setting circuits with or from the data lines corresponding to the current setting circuits electrically, wherein

currents for generating the compensation currents (currents for setting the compensation currents) are supplied from the current source to the current setting circuits in a state in

which the current setting circuits and the data lines corresponding to the current setting circuits are electrically broken.

Moreover, an active matrix display apparatus of the present invention includes:

a pixel circuit unit (**1**) in which electro-optic elements (EL) luminance of which changes according to flowing currents and pixel circuits (**110**, **120**) for generating drive currents to be supplied to the electro-optic elements are arranged in a matrix;

a current source for supplying a writing current (Idata**1**) to each of the pixel circuits through a plurality of data lines;

a current setting circuit (**130**) provided to each of said data lines for flowing a compensation current in each data line into a direction of cancelling the writing current; and

a switch (M**5**) connecting or breaking the current setting circuit with or from a data line corresponding to the current setting circuit electrically, wherein

a current for generating the compensation current (a current for setting the compensation current) is supplied from the current source to the current source setting circuit in a state in which the current setting circuit and the data line corresponding to the current setting circuit is broken by the switch.

It is preferable that the current source setting circuit includes a holding capacitor (C**1**) holding a voltage obtained by converting the current supplied from the current source, and a transistor (M**1**) for supplying a current according to the voltage held by the holding capacitor to the data line as the compensation current.

In the present invention, a current (Idata**2**) having a magnitude obtained by subtracting the compensation current (Iz) from the writing current (Idata**1**) supplied from the current source is supplied to the pixel circuits.

According to the present invention, the influences of the parasitic capacitance of a data line can be suppressed, and the writing operation of current can be stabilized.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a diagram showing an example of the configuration of pixel circuits and a zero current setting circuit according to a first embodiment of the present invention;

FIG. **2** is a timing chart for illustrating the operation of the pixel circuits and the zero current setting circuit according to the first embodiment of the present invention;

FIG. **3** is a configuration diagram showing the configuration of an active matrix field emission display apparatus according to the present invention;

FIG. **4** is a diagram showing the configurations of pixel circuits and a zero current setting circuit of a comparison example; and

FIG. **5** is a diagram showing an example of the configuration of pixel circuits and a zero current setting circuit according to a second embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

In the following, the preferred embodiments of the present invention are described in detail with reference to the attached drawings.

First Embodiment

FIG. **3** is a configuration diagram showing the configuration of an active matrix field emission display apparatus according to the present invention.

In FIG. **3**, a reference numeral **1** denotes a pixel circuit unit composed of pixel circuits arranged in a matrix. In the pixel circuit unit **1**, electroluminescent elements and circuits driving the electroluminescent elements are arranged in a matrix, and the pixel circuit unit **1** includes scanning signal lines connecting them in row directions and data lines connecting them in column directions.

A reference numeral **2** denotes data line switches performing the separation and the connection of the data lines. A reference numeral **3** denotes a zero current setting circuit provided to each pixel circuit column into which a current is written based on a zero setting current (a reference current). A reference numeral **4** denotes column current control circuits supplying line-sequential data line current signals Idata and zero setting currents to the data lines connected with pixel circuit groups arranged in the column directions. A reference numeral **5** denotes a column scanning circuit connected to the column current control circuits **4** for supplying the line-sequential data line current signals Idata to the data lines.

The column current control circuits **4** are variable current sources. The column current control circuits **4** generate currents based on data, and supply the generated currents to the plurality of pixel circuits in the column directions, which are connected to the column current control circuits **4** with the data lines. The column current control circuits further generate zero setting currents independent of data, and supply the generated zero setting currents to the zero current setting circuits **3**.

The column scanning circuit **5** samples three image signals of R, G and B input into the column current control circuits **4** to each column.

A reference numeral **6** denotes a row scanning circuit connected to the pixel circuits arranged in the row directions, and sequentially outputs line scanning signals P**1***m* and P**2***m* to each line (a letter m denotes an integer of (1-M) on the supposition that there are M row scanning signal lines). Because each pixel circuit includes two row selection signal lines in the examples of the pixel circuits shown in the following embodiments, it is supposed that two row scanning signals also exist here. However, there can be cases where each pixel circuit includes one, three or the like of row selection lines in addition to the case of two row selection lines.

FIG. **1** shows a current programming circuit according to a first embodiment of the present invention. The current programming circuit **100** of the present embodiment includes a first row pixel circuit **110**, a second row pixel circuit **120** (although pixel circuits are continuously arranged in a third row, a fourth row and so forth after the second row pixel circuit **120**, the illustration of them is omitted in FIG. **1**), and a zero current setting circuit **130**. Although only a part of the current programming circuit **100** connected to one data line is shown in FIG. **1**, it is needless to stay that the matrix display apparatus of FIG. **3** includes a plurality of data lines and the same current programming circuit is provided to each data line.

FIG. **2** is a timing chart for illustrating the operation of the circuit of FIG. **1**. The ordinate axes of FIG. **2** indicate the voltage values of each signal, and the abscissa axes of FIG. **2** indicate times. The signal input into each of signal lines L, P**1***z*, P**2***z*, . . . of FIG. **1** is denoted by the same marks as those in FIG. **1**.

In the present specification, a data line **150** indicates only a part to which the pixel circuits **110**, **120**, . . . are commonly connected, and the data line **150** is distinguished from wiring **160** on a current source side from a switch M**5**.

A reference mark Idata**1** in FIG. **2** denotes a current flowing through the wiring **160** connected to the column current con-

trol circuits **4**, not shown in FIG. **1**, on the left side from a supply port of a current Iz generated by the zero current setting circuit **130**. The reference mark Iz denotes the output current of the zero current setting circuit **130**, and a reference mark Idata**2** denotes a current flowing through a part nearest to the switch M**5** of the data line.

FIG. **4** is a diagram showing the configuration of a current programming circuit as a comparison example.

Although the configurations of the pixel circuits **110** and **120** and the zero current setting circuit **130** of the comparison example shown in FIG. **4** are the same as those shown in FIG. **1**, the configuration of the comparison example does not include the data line switch M**5** between the zero current setting circuit **130** and the first row pixel circuit **110**. The configuration of the comparison example differs from that shown in FIG. **1** in that the data line **150** portion, to which each of the pixel circuits **110**, **120**, . . . are connected, is continuous to the wiring **160** portion of the zero current setting circuit **130**.

First, for making it easy to understand, the configuration and the operation of the comparison example, which is not provided with the data line switch M**5**, is described using FIGS. **2** and **4**.

Now, the operation of the first row pixel circuit connected to a certain data line is considered. When the row scanning signal P**11** becomes a high level in FIG. **2**, an nMOS transistor M**7** used as a switch for a first program (row selection) is turned on, and a pMOS transistor M**9** as a switch for light emission selection turns off. Moreover, when the row scanning signal P**21** becomes the high level, an nMOS transistor M**6** used as a switch for a second program turns on.

As a result, the image data current Idata**2** flowing through the data line is led to the gate and the drain of a pMOS transistor M**8** used as a drive transistor, and charges a capacity C**2** connected between the gate and the source.

The voltage of the capacity C**2** connected to the gate of a pMOS transistor M**8** used as a switch for drive is set as a gate-source voltage sufficient for the current driving the electroluminescent element (field luminescent element) EL based on the image data current flowing through the data line to flow through the pMOS transistor M**8**. Next, when the row scanning signal P**21** becomes a low level, the nMOS transistor M**6** used as the switch for the second program turns off, and the voltage of the capacity C**2** is held. The period until now is a first row current setting period (drive current programming period).

After that, when the row scanning signal P**11** becomes the low level, the nMOS transistor M**7** used as the switch for the first program (row selection) turns off, and the pMOS transistor M**9** used as the switch for the light emission selection turns on. The supply of a drive current to the electroluminescent element EL is controlled by the gate potential of the transistor M**8** for drive, and the current flowing through the electroluminescent element EL is controlled. A period during which the electroluminescent element EL is emitting light (is not emitting light in case of a black display) is a light emitting period. Moreover, when the first row current setting period ends, a second row current setting period begins, and a drive current is sequentially written in the current setting period of each row based on an image data signal.

By the way, although it is preferable that the current of a line-sequential data line current signal is zero in the minimum luminance (black) display, it is actually difficult to make the current zero owing to the circuit configuration. Even if the image data input into one of the column current control circuits **4** of FIG. **3** is made to a black display signal, that is even if the signal voltage is made to the black display voltage level, the output current of the column current control circuit **4** does not become zero completely, and a little current (called as a zero current) flows through the connected wiring **160**. If the current of the line-sequential data line current signal does not become zero, it is impossible to make the drive current of the electroluminescent element EL zero, and the setting of the black display cannot be performed sufficiently. Moreover, because the zero current is different at each data line owing to the dispersion of the column current control circuits **4**, it is difficult to perform the subtraction of the zero current uniformly.

The inventors of the present application have paid attention to the problem previously, and proposed a method of providing the zero current setting circuits for performing the setting of the black display correctly (Japanese Patent Application Laid-Open No. 2004-312015). This patent application proposed a current programming circuit **100** including a zero setting circuit **130** as shown in FIG. **4**. A zero current is programmed in the zero current setting circuit **130** in a predetermined period (the period is called as a zero current setting period) in a vertical blanking period. In a current programming period of the pixel circuits **110**, **120**, etc., a current is supplied from the zero current setting circuit into the data line in the direction of cancelling the current from column current circuits.

During the zero current setting period, the image data inputted into one of the column current control circuits **4** of FIG. **3** is made to a black display signal. That is, the signal voltage is made to be the black display voltage level.

As stated above, the output current of the column current control circuit **4** does not completely become zero, but a zero current flows through the connected wiring **160**. Here, the control signals P**1***z* and P**2***z* are made to be the high level to turn nMOS transistors M**3** and M**2** on, respectively, the zero current flow into the zero current setting circuit **130** and the voltage across a capacity C**1** connected to the gate of a pMOS transistor M**1** is set as a level correlated to the zero current. When the control signals P**1***z* and P**2***z* become the low level, the voltage of the capacity C**1** is held.

In the scanning period, a current Iz which is determined by the voltage across the capacity C**1** flows through the pMOS transistors M**1** and M**4**. The current flows into the data line, where a data current Idata**1** has been supplied from column current circuit. Since the current Iz on the data line cancels a part of the data current Idata**1**, current Idata**2** to be supplied to pixel circuits satisfies the formula of Idata**2**=Idata**1**−Iz.

Consequently, as the zero current is canceled, it becomes possible to set the current to flow in the pixel circuits completely zero at the time of a black display. Thus, by providing the zero current setting circuits, it becomes possible to set the true black displays.

However, the inventors of the present application have found that, even if the setting of the current is tried to be performed by the zero current setting circuits, it is difficult to stably perform the zero current setting owing to the influences of parasitic capacitance Cx of the data lines. Hereafter, the problem is described.

In FIG. **1**, the parasitic capacitance Cx of a data line is shown. The capacity Cx results from wiring capacity, the capacity between the gate and the source of the transistor of the pixel circuits connected to a data line, and the like. Because the zero setting current is a minute current, it is not always easy to write a current based on the zero setting current during a limited vertical blanking period even if the current is tried to be set with the zero current setting circuit when the influences of the parasitic capacitance of the data line are exerted.

For example, it is supposed that pixel circuits from the first to the nth rows are connected to a certain data line, and that the voltage across the capacity C2 of the nth pixel circuit is set to be high for setting the nth pixel circuit to be high luminance. Then, the potential of the data line, or the voltage across the parasitic capacitance Cx, becomes low. In the zero current setting period in the next frame, it becomes difficult to fully raise the potential of the capacity C1 of the zero current setting circuit. This is because the zero current setting is the minute current writing operation and the zero current setting period is finite.

Furthermore, the potential of the data line is high in the case where the nth pixel has been black display and the potential of the data line is low in the case where the nth pixel has been high luminance. A difference is caused between the potentials of the data line in these two cases, which makes performing the zero current setting unstable.

In order to solve the problem, as shown in FIG. **1**, the inventors of the present application have devised to provide the switch M5 of an nMOS transistor between the data line **150** and the current output terminal of the zero current setting circuit **130**, and to turn the switch M5 on and off with the control signal on the signal line L. Then, the inventors have devised to turn off the switch M5 during the zero current setting period for separating the data line and the pixel circuits **110**, **120**, . . . from the zero current setting circuit **130**. Thereby, the zero current is separated from the parasitic capacity of the data line during the zero current setting period to make it possible to write the zero current into the zero current setting circuit correctly. Moreover, because the zero current is not influenced by the parasitic capacitance, the writing of the zero setting current can be performed more quickly.

Although the capacity C1 may be individually formed as a capacity element, the capacity C1 also may not be formed as an element, but the parasitic capacitance formed between the gate and the source (the capacity of the overlapping of the gate electrode and the source region, or the like) may be used as capacity C1.

Second Embodiment

FIG. **5** is a diagram showing an example of the configuration of the current programming circuit according to a second embodiment of the present invention. In the present embodiment, the configuration of the zero current setting circuit **130** is more simplified by omitting the nMOS transistor M3 and the pMOS transistor M4, and by connecting the PMOS transistor M1 to the data line directly. In such a configuration, also the effect similar to that of the first embodiment also can be acquired.

Although the active matrix type display apparatus using the current based driven display elements is picked up to be described as an example of using the current programming apparatus according to the present invention above, the current programming apparatus according to the present invention can be applied to a use, as long as the use is that using a current setting circuit holding a current to be flown into a data line as the gate-source voltage of a transistor. The use of the current programming apparatus according to the present invention is not limited to the active matrix type display apparatus using the current based driven display elements such as electroluminescent elements and electron emitting elements, but the current programming apparatus according to the present invention is used as a circuit for current programming such as an analog memory. In case of using the current programming apparatus as the analog memory, the current programming apparatus adopts a configuration in which the electroluminescent element EL is removed from each of the pixel circuits, and analog value is taken out from the circuit as a current value. Moreover, the application of the present invention is not restricted to the matrix-like display apparatus, but the present application can be applied also to a line-like display apparatus.

The present invention is used for an active matrix type display apparatus of a current based driven type light emitting devices such as the electroluminescent elements (EL elements) and other electro-optic elements, and also used for an analog memory.

This application claims priority from Japanese Patent Application No. 2004-342129 filed Nov. 26, 2004, which is hereby incorporated by reference herein.

What is claimed is:

1. A matrix type display apparatus, comprising:

a pixel circuit unit including electroluminescent elements and pixel circuits, driving the electroluminescent elements arranged in a matrix;

a plurality of data lines, each corresponding to a column of the pixel circuits, for supplying a data current to the pixel circuits;

predetermined current setting circuits for supplying to the data lines a predetermined current for reducing a current to be supplied to the data lines, according to a setting by a reference current unrelated to a displaying, at a time of black displaying of the electroluminescent elements;

switches, corresponding to each of the data lines, arranged between the pixel circuit unit and the predetermined current setting circuits, and

a row scanning circuit for controlling on and off of the switches, wherein

the row scanning circuit turns off the switches to disconnect the pixel circuit unit and the predetermined current setting circuits, and sets the predetermined current in the predetermined current setting circuits, and

thereafter, the row scanning circuit turns on the switches to connect the pixel circuit unit and the predetermined current setting circuits, and to supply the data lines with the data currents and the predetermined current, wherein

the switches are separate from the pixel circuit unit.

2. A matrix type display apparatus according to claim **1**, wherein the predetermined currents are currents generated by said current source when said display elements are displayed at their minimum luminance.

3. A matrix type display apparatus according to claim **1**, wherein said display elements are electroluminescence elements.

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专利名称(译)	电流编程装置和矩阵型显示装置		
公开(公告)号	US7969392	公开(公告)日	2011-06-28
申请号	US11/283862	申请日	2005-11-22
[标]申请(专利权)人(译)	佳能株式会社		
申请(专利权)人(译)	佳能株式会社		
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IPC分类号	G09G3/30 G09G3/10		
CPC分类号	G09G3/325 G09G2320/043 G09G2320/029 G09G2300/0861		
优先权	2004342129 2004-11-26 JP		
其他公开文献	US20060114195A1		
外部链接	Espacenet USPTO		

摘要(译)

一种矩阵型显示装置，包括：像素电路单元，包括电致发光元件;像素电路，驱动以矩阵排列的电致发光元件;多条数据线，每条数据线对应于一列像素电路，用于向像素电路提供数据电流，预定电流设定电路，用于在黑色显示电致发光元件时，根据与显示无关的参考电流的设定，向数据线提供预定电流，以减小要提供给数据线的电流。另外，对应于像素电路和预定电流设置电路之间的每条数据线布置开关，并且行扫描电路控制开关的接通和断开。行扫描电路断开开关以断开像素电路单元和预定电流设定电路，并在预定电流设定电路中设定预定电流，此后，行扫描电路接通开关以连接像素电路单元和预定电流设定电路，并向数据线提供数据电流和预定电流。